CLAIMS

1. An apparatus comprising:

an analysis block configured to generate debug information in response to (i) a command input, (ii) one or more simulation outputs, and (iii) one or more compiler outputs;

a graphical user interface configured (i) to present said command input in response to one or more user input parameters and (ii) to display said debug information; and

a memory circuit configured to store said one or more simulation outputs and said one or more compiler outputs.

2. The apparatus according to claim 1, wherein said one or more user input parameters comprise identification of a memory address.

3. The apparatus according to claim 1, wherein said one or more user input parameters comprise identification of specific memory accesses.

4. The apparatus according to claim 1, wherein said one or more user input parameters comprise one or more of a command for

expanding the display of a memory map, a command for retrieving information related to accesses to said memory map, a command for retrieving assembly code related to particular accesses and one or more commands related to filtering operations.

5. The apparatus according to claim 1, wherein said one or more simulation outputs comprise information from one or more of a processor simulator and one or more processor simulation models.

6. The apparatus according to claim 1, wherein said graphical user interface is configured to present said debug information in one or more windows.

7. The apparatus according to claim 1, wherein said graphical user interface is configured to present said debug information in one or more frames.

8. The apparatus according to claim 1, wherein said one or more user input parameters are entered using one or more of a mouse, a keyboard, a touch screen and voice recognition.

9. The apparatus according to claim 8, wherein said graphic user interface is configured to provide an indication of receipt of said user input parameters.

10. A method for debugging RTL simulations of processor based system on chip (SoC) comprising the steps of:

(A) identifying a memory address to be examined;

(B) retrieving one or more accesses related to said memory address;

(C) identifying a specific one of said one or more accesses to be examined; and

(D) retrieving one or more types of debug information related to said identified access.

11. The method according to claim 10, wherein said one or more types of debug information comprise one or more assembler instruction codes.

12. The method according to claim 10, wherein said one or more types of debug information comprise a register status of said processor.

13. The method according to claim 11, wherein said one or more types of debug information comprise a program flow leading to said one or more assembler instruction codes.

14. The method according to claim 10, wherein said one or more types of debug information comprise a program structure.

15. The method according to claim 10, wherein retrieving one or more accesses related to said memory address comprises:

responding to activation of a button presented by a graphic user interface.

16. The method according to claim 10, wherein identifying a specific access is performed via a graphic user interface.

17. The method according to claim 10, wherein retrieving one or more types of debug information is performed in response to a button of a graphic user interface being actuated.

18. The method according to claim 10, further comprising the step of:

displaying said retrieved one or more accesses and said retrieved one or more types of debug information using a graphic user interface.

19. The method according to claim 18, further comprising the step of:

modifying information displayed using said graphic user interface in response to one or more filter commands.

20. An apparatus comprising:

means for identifying a memory address in a user defined memory map;

means for retrieving one or more accesses related to an identified memory address from simulation results;

means for identifying a specific access to be examined;

means for retrieving one or more types of debug information related to said specific access from said simulation results.